

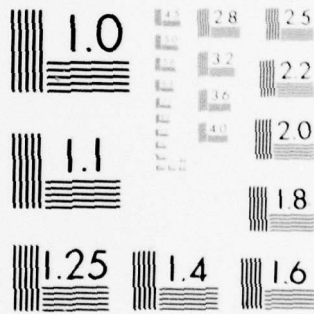
AD-A077 845 BURROUGHS CORP PAOLI PA FEDERAL AND SPECIAL SYSTEMS GROUP F/G 9/2
MODULAR SYSTEM CONTROL DEVELOPMENT MODEL (MSCDM). DESIGN SPECIF--ETC(U)
AUG 79 DCA100-76-C-0083
UNCLASSIFIED 66160 SBIE-AD-E100 305 NL

| OF |

AD
A077845



END
DATE
FILMED
1-80
DDC



MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

AD-E100 305

11

66160

August 1979

LEVEL

DDC
RECEIVED
DEC 3 1979
REGISTRY
E

DESIGN SPECIFICATION
FOR THE
MODULAR SYSTEM CONTROL
DEVELOPMENT MODEL (MSCDM)

for

THE DEFENSE COMMUNICATIONS AGENCY
WASHINGTON, D.C. 20305

DDC FILE COPY

This document has been approved
for public release and sale; its
distribution is unlimited.

Burroughs Corporation

Federal and Special Systems Group

Paoli, Pa. 19301

AD A 077845

REPORT DOCUMENTATION PAGE

READ INSTRUCTIONS
BEFORE COMPLETING FORM

1. REPORT NUMBER

2. GOVT ACCESSION NO.

3. RECIPIENT'S CATALOG NUMBER

14 66160

4. TITLE (and Subtitle)
~~Design Specification for the~~ Modular System
Control Development Model (MSCDM).
Design Specification. A077844

5. TYPE OF REPORT / PERIOD COVERED

9 FINAL Sep 76 - Nov 79.

6. PERFORMING ORG. REPORT NUMBER

7. AUTHOR(s)

8. CONTRACT OR GRANT NUMBER(s)

15 DCA100-76-C-0083

9. PERFORMING ORGANIZATION NAME AND ADDRESS

Burroughs Corporation
Federal and Special Systems Group
Paoli, PA 19301

10. PROGRAM ELEMENT, PROJECT, TASK
AREA & WORK UNIT NUMBERS

PE 33126
T&CCP 3012 Task 15203

11. CONTROLLING OFFICE NAME AND ADDRESS

Defense Communications Agency
Defense Communications Engineering Center
1860 Wiehle Ave., Reston, VA 22090

12. REPORT DATE
11 August 1979

13. NUMBER OF PAGES
50

14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office)

15. SECURITY CLASS. (of this report)

12 52 UNCLASSIFIED

15a. DECLASSIFICATION/DOWNGRADING
SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for Public Release; Distribution Unlimited

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

18 SBIE

19 AD-E100 305

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Ring Network
Loop Network
System Control Modules

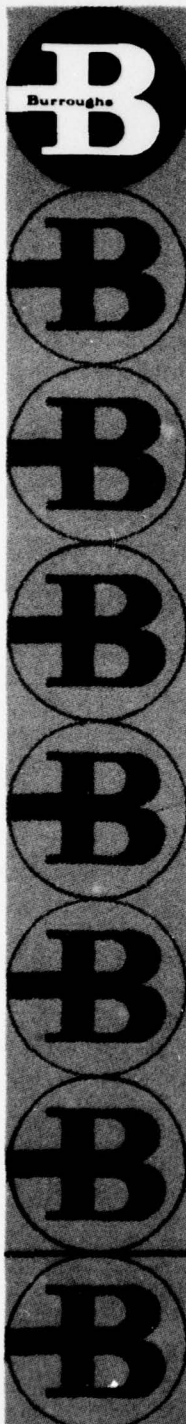
Exploratory System Control Model
(ESM)

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The physical specification of the MSCDM and its relationship to the existing Exploratory System Control Model (ESM) is described. The physical placement and operation of each hardware module is described. A description of each software module is also provided presenting intermodule connectivity specifics.

070 040 The
79 11 20 1003
UNCLASSIFIED

August 1979



**DESIGN SPECIFICATION
FOR THE
MODULAR SYSTEM CONTROL
DEVELOPMENT MODEL (MSCDM)**

for

**THE DEFENSE COMMUNICATIONS AGENCY
WASHINGTON, D.C. 20305**

DISTRIBUTION STATEMENT A

Approved for public release;
Distribution Unlimited

Burroughs Corporation

Federal and Special Systems Group

Paoli, Pa. 19301

Contents

| <u>Section</u> | <u>Page</u> |
|--|-------------|
| 1. System Configuration | 1 |
| 1.1 Relationship with ESM Loops 1-4 | 3 |
| 1.2 Module Intercommunication | 5 |
| 2. Hardware | 6 |
| 2.1 Program Development Unit | 9 |
| 2.2 Loop 5 Cabinet Hardware | 11 |
| 3. Software | 21 |
| 3.1 MSCDM Functions | 21 |
| 3.2 Distributed Master Control Program | 35 |
| 3.3 User Language | 44 |
| 3.4 System Utilities | 46 |
| 3.5 Diagnostics | 47 |

List of Figures

| <u>Figure</u> | | <u>Page</u> |
|---------------|---------------------------------------|-------------|
| 1 | MSCDM System Configuration | 2 |
| 2 | ESM Multiloop Network | 4 |
| 3 | Logic and Placement | 7 |
| 4 | PDP 11/V03 | 10 |
| 5 | Control Panels | 14 |
| 6 | H9270 Backplane Card Positions | 16 |
| 7 | H9270 Backplane Card Positions - FIAC | 17 |
| 8 | Microcomputer Backplane - SIG | 18 |
| 9 | Controls on Logic Cards | 20 |
| 10 | Input from Loop Flow Control | 37 |
| 11 | Input from Exodevice Flow Control | 40 |
| 12 | DMCP Idle Flow Control | 40 |

| | |
|--------------------|--|
| Accession For | |
| NTIS GPO&I | <input checked="checked" type="checkbox"/> |
| DOC TAB | <input type="checkbox"/> |
| Unannounced | <input type="checkbox"/> |
| Justification | <input type="checkbox"/> |
| By _____ | |
| Distribution/ | |
| Availability Codes | |
| Dist | Avail and/or special |
| A | |

DESIGN SPECIFICATION FOR THE FEASIBILITY DEVELOPMENT MODEL

1. System Configuration

The MSCDM Feasibility Development Model (FDM) is given in Figure 1. The loop will be referred to as loop 5 in the ESM Multiloop Network. The default MSCDM functions are assigned to each node as shown; however, since each node is down line loadable from the program development unit (PDU), functions can be mapped to hardware modules in many different configurations. Each node is assigned a node designator as shown. Each node owns at least one logical identifier (LID) which is equal to its node designator (ND). Thus packets can be addressed to any node in the system by setting the destination LID to the ND of that node. The indirect method of addressing using LID/functional address (FAD) conversion tables used for ESM will also be used in the MSCDM. Thus any MSCDM node can communicate with any ESM node. In addition the terminal node (ND=25) will have the ESM ATTACH capability so that it can communicate with ESM terminals and host processors.

The Loop Interface Units (LIU) are the same as in ESMD Loop 4. Thus the loop is actually a double loop configuration with the same ESMD loop-back capability. The microcomputers are DEC LSI-11 micro-computers with 32K x 16 memories. The PDU is a PDP11V03 system which is housed in its own cabinet with power supply and can be used independently of the loop. The PDU can be used as a general purpose processor. The loop is contained in a separate cabinet with power supply.

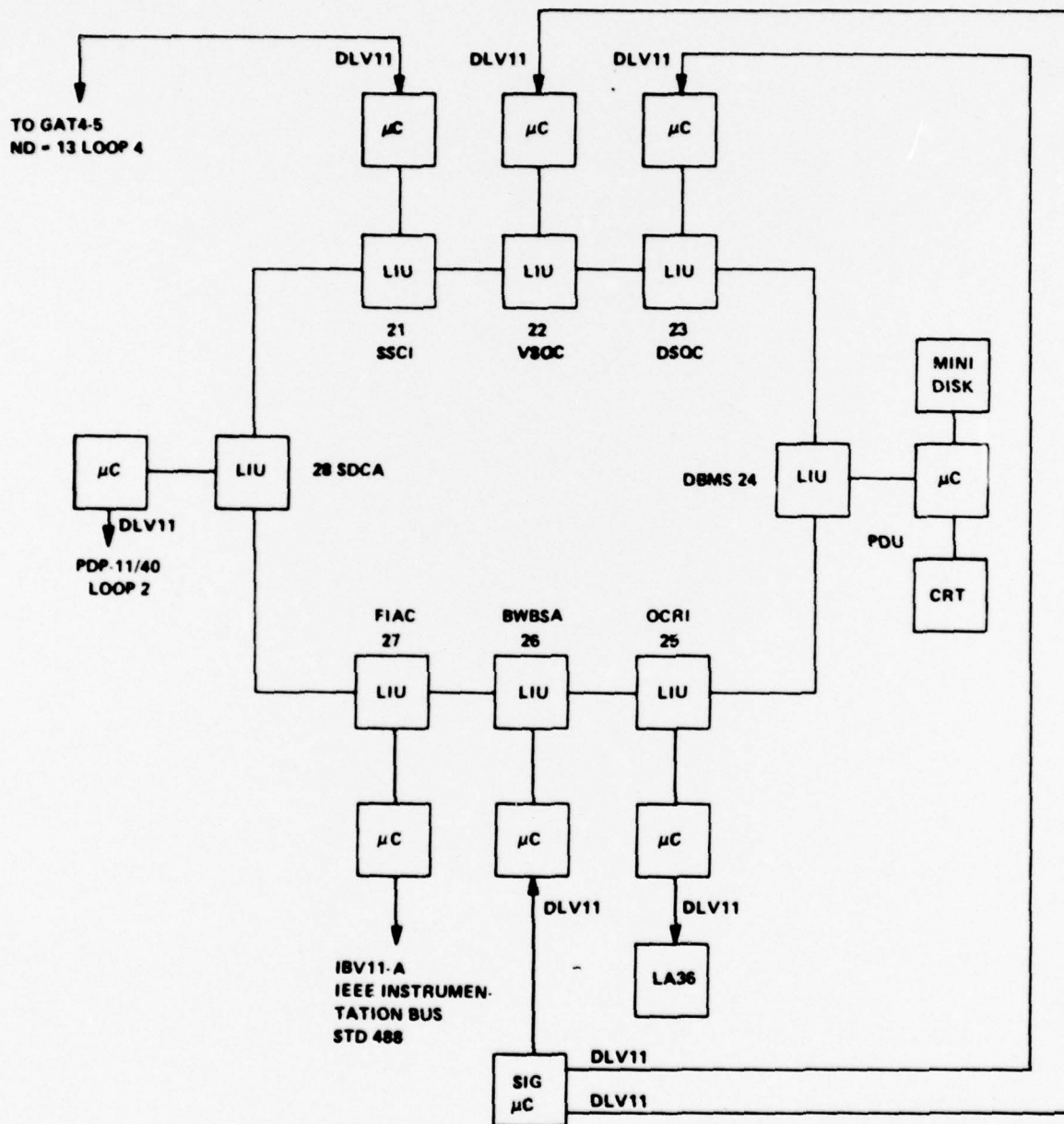


Figure 1. MSCDM System Configuration

An IEEE 488 interface is provided at node 27. Node 28 contains a serial interface that is cable connected to the serial interface in the PDP11/40 HSTB (ND=5) in loop 2. Thus the MSCDM appears as a terminal to HSTB.

Simulated inputs to nodes 22 (VSQC), 23 (DSQC), and 26 (BWBSA) will be generated by a LSI-11 microprocessor used as a simulated input generator (SIG). The SIG will contain three serial interfaces that connect to DLV11 interfaces in nodes 22, 23 and 26.

1.1 Relationship with ESM Loops 1-4

The MSCDM will be integrated as loop 5 of the ESM Multiloop Network shown in Figure 2. Any node has the capability to communicate with any other node in the network. Any terminal has the capability to ATTACH itself to any node. The MSCDM loop 5 can operate independently of the other loops or can be used with the other loops. Loop 5 has a gateway connection to loop 4, and a connection to the PDP11/40 in loop 2. The loop 5 microprocessor interfaced to the PDP11/40 appears as a terminal to the PDP11/40 operating system.

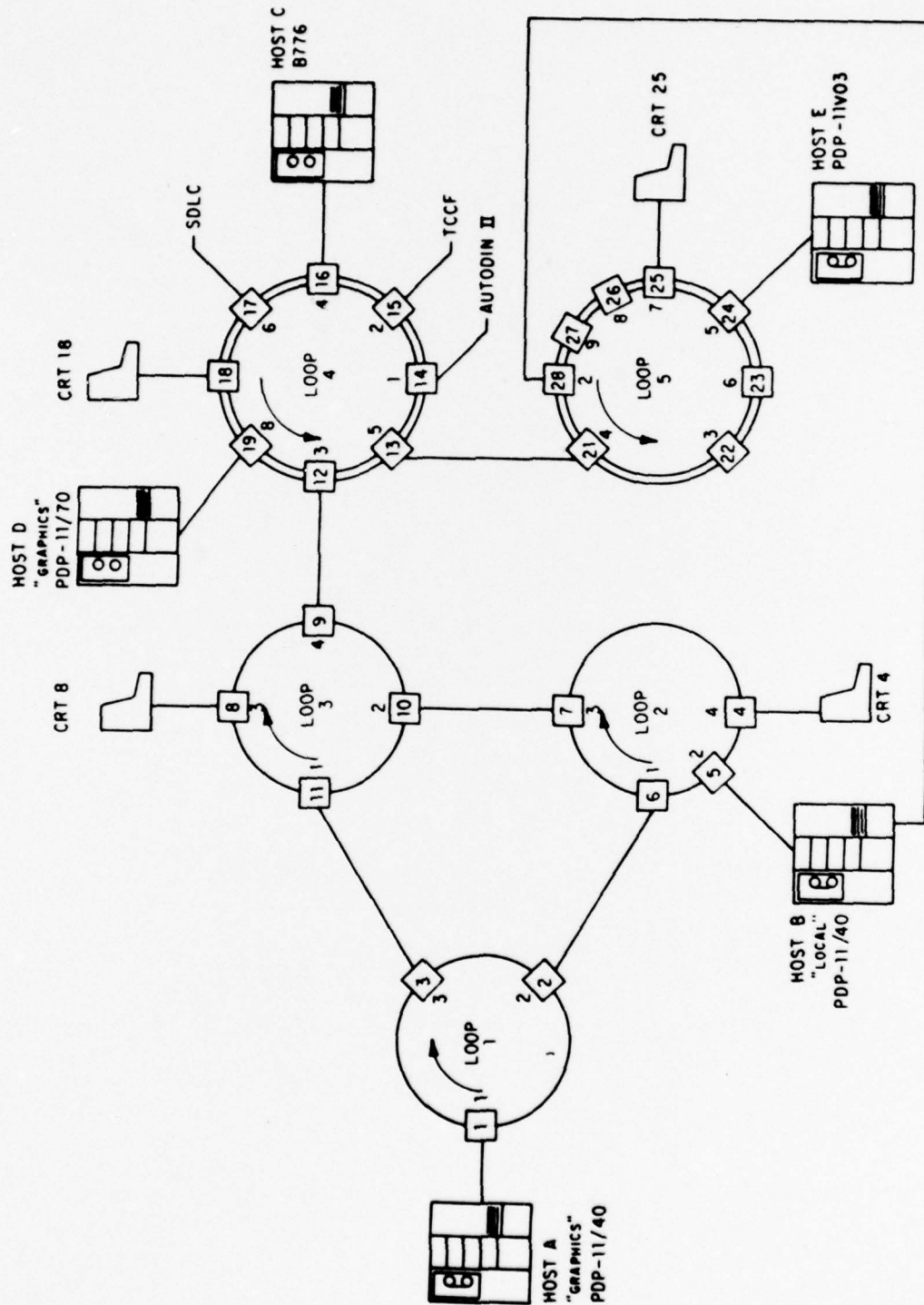


Figure 2. ESM Multiloop Network

1.2 Module Intercommunication

Any nodal module can communicate with any other module, however the nodal software for the MSCDM application defines the flow of information in the system. The OCRI terminal is normally ATTACHED to the DBMS which runs the User Language. The other ESM terminals communicate with the User Language via the loop 4-5 gateway (SSCI).

The SIG generates inputs to the VSQC, DSQC and BWSBA, who communicate faults to the FIAC module. FIAC generates event reports to the OCRI and DBMS. The PDP11/40 in loop 2 generates inputs to the SDCA which generates fault reports to the OCRI and DBMS. The DBMS, OCRI and FIAC communicate with the other loops via SSCI.

An LA36 DECWriter will be used as the OCRI hard-copy terminal attached to node 25. A VT52 DECSCOPE will be used as a local CRT terminal connected to the Program Development Unit (PDU).

2. Hardware

The MSCDM Loop 5 system consists of the following major physical entities:

- PDP11V03 Program Development Unit (PDU) consisting of LSI-11 processor and mini-disk
- Loop 5 consisting of 8 nodes and simulated input generator (SIG) processor
- CRT Terminal VT52
- LA36 Printer Terminal

Loop 5 is contained in a cabinet with power supply and operator controls. The loop 5 cards are contained in backplanes as shown in Figure 3. The PDP 11V03 PDU is contained in a separate cabinet.

A list of MSCDM hardware deliverables is given in Table 1.

| | | | |
|------------|------------|------------|------------|
| NODE 21 | NODE 22 | NODE 23 | SIG GEN |
| SSCI | VSQC | DSQC | |
| FANS | | | |
| NODE 28 | NODE 27 | NODE 26 | NODE 25 |
| SDCA | FIAC | BWBSA | OCRI |

| | | | | |
|-----|---------|---|---------|--|
| FAN | SPARE | | BUS CTL | |
| | LIU | - | 28 | |
| | LIU | - | 27 | |
| | LIU | - | 26 | |
| | LIU | - | 25 | |
| | LIU | - | 24 | |
| | LIU | - | 23 | |
| | LIU | - | 22 | |
| | LIU | - | 21 | |
| | CLK BUF | | CLK GEN | |
| FAN | | | | |

VIEWING
COMPONENTS
↓

Figure 3

Logic Card Placement
(Card insertion view)

Table 1--HARDWARE DELIVERABLES

| <u>Style No.</u> | <u>Manufacturer</u> | <u>Description</u> | <u>Quantity</u> |
|------------------|---------------------|-------------------------------|-----------------|
| PDP-11V03 | Digital Equip Co | Program Develop- ment Unit | 1 |

(SR-VXRRA-LA consisting of :

System w/LSI-11 CPU
16Kx16 MOS RAM
Bootstrap Loader
Serial Line Interface
Cable
Dual Drive Floppy Disk
w/512KB Capacity
Disk Interface
Cabinet Assembly
LA-36 Decwriter
RT-11 Real Time OS)

| | | | |
|------------------|------------|---------------------|----|
| QJ925-AY | DEC | FORTTRAN | 1 |
| MSV11-CA | DEC | 16Kx16 MOS RAM | 1 |
| BAll-ME | DEC | Expander Box | 1 |
| BCV1B-02 | DEC | Cable | 1 |
| VT52 | DEC | Decscope CRT | 1 |
| DLV11 | DEC | Serial Intf Card | 1 |
| BC05M-2C | DEC | Cable | 1 |
| KD11-HD-LSI-11/2 | DEC | CPU plus 32Kx16 RAM | 8 |
| MRV11-AA | DEC | PROM Ldr Card | 8 |
| DLV11 | DEC | Serial Intf Card | 10 |
| IBV11-A | DEC | IEEE 488 Std Intf | 1 |
| H9270 | DEC | 4x4 Backplane | 8 |
| DL11 | DEC | Synchronous Intf | 1 |
| LIU | Burroughs | Loop Intf Card | 8 |
| BLIUI | Burroughs | Q-Bus to LIU Intf | 8 |
| CLK GEN | Burroughs | Clk Gen Card | 1 |
| CLK BUF | Burroughs | Clk Buffer Card | 1 |
| BUSCTL | Burroughs | Bus Control Card | 1 |
| ASYNCH | Burroughs | Serial Intf Card | 1 |
| UPAN | Burroughs | Utility/Cntl Panel | 1 |
| OPAN | Burroughs | Operator Panel | 1 |
| B700 Style | Burroughs | Disk Cab & Hardware | 1 |
| N/A | Burroughs | MSCDM Bkplane Assy | 1 |
| #SW-12H | Power/Mate | 12V/22A Switchng PS | 1 |
| #SW-5K | Power/Mate | 5V/120A Switchng PS | 1 |

2.1 Program Development Unit

The Program Development Unit (PDU) makes up Node 24. Software development is done on the PDU for all eight microcomputer modules. The PDU hardware is listed below:

- SRRVXRRRA-LA System with LSI-11 CPU, 16k x 16 MOS RAM, bootstrap loader, serial line interface, cable, dual drive floppy disk with 512k byte capacity, disk interface, cabinet assembly, LA36 DECWriter, and RT-11 real-time operating system.
- QJ925 -AY FORTRAN
- MSV11-CA 16k x 16 MOS RAM
- BA11-ME Expander Box
- BCV1B-02 Cable
- VT52-AA DECSCOPE CRT
- DLV11 Serial Interface
- DCO5M-2C Cable

The backplane card layout is given in Figure 4.

VIEWING COMPONENTS

| | | |
|--|-------------------------------|---|
| KD11-J-LSI-11 (CPU) (M7264-QUAD) | | 1 |
| BLIUI | | 2 |
| MSV11-CD | 16KW (MEMORY) (M7955-QUAD) | 3 |
| BCV1B (Bus Expansion Card) (M7946) | | 4 |

UPPER BACKPLANE

VIEWING COMPONENTS

| | | |
|-------------------------------|-------------------------------|---|
| BCV1B (Bus Expansion Card) | DLV11 (SLU) M8028/M7940) | 1 |
| MSV11-CD | 16KW (MEMORY) (M7955-QUAD) | 2 |
| REV11-A (ROM) (M9400YA) | | 3 |
| | | 4 |

LOWER BACKPLANE

Figure 4
PDP 11/VO3
Node 24 PDU

2.2 Loop 5 Cabinet Hardware

The loop consisting of Loop Interface Units (LIUs) connected together, resides entirely within the confines of the MSCDM cabinet. All LIUs are located in a specially constructed logic card backplane which has room for ten double card slots. Three of the single card slots in this backplane are used for the following three functions: Clock Generation (CLK GEN); Clock Buffering (CLK BUF); and LSI-11 Bus Control (BUSCNTL).

Each loop node is made up of a standard set of logic cards:

- LSI-11 DEC CPU
- 64KB DEC RAM Memory
- 8KB DEC PROM Memory
- BLIUI Burroughs Q-Bus to LIU Interface
- LIU Burroughs Loop Interface Unit
- DIU Device Interface Unit

This standard set of logic cards is not always entirely resident inside the MSCDM cabinet as is the set of loop interface units. The exception, for the case of the equipment involved in the MSCDM system is the node connecting the PDP11/V03 Program Development Unit to the loop. In this case, all of the standard logic cards for this node (except the LIU) reside within the LSI-11 backplane internal to the PDP11/V03. The PDU connection to the Loop 5 is a cable between the LIU, residing in the Burroughs backplane (in the MSCDM cabinet), and the BLIUI, residing in the LSI-11 backplane inside the PDP11/V03.

The other seven node card sets making up Loop 5 are resident in the MSCDM cabinet. With the exception of the LIUs, the node cards are contained in the individual DEC card backplanes. The 7 DEC backplanes are mounted in the cabinet in a 4 x 2 assembly (i.e. two rows of four DEC H9270 backplanes) which occupies the central and middle-to-left position of the cabinet, when viewed from the card insertion side. The eighth LSI-11 microcomputer included in the 4 x 2 cluster is used for the SIG function (Simulated Inputs Generator).

An operator's panel exists on the top front of the cabinet. This panel has. a control switch for AC POWER ON/OFF; a control switch for LOOP CLEAR; and eight node RUN LEDs (that indicate a cycling CPU).

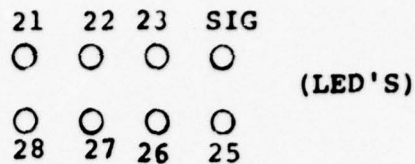
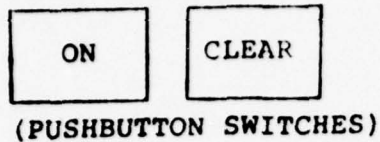
A Utility panel also exists inside the front door of the MSCDM cabinet. The main power is split between two circuit breakers that are mounted on the left side of this panel. Cabinet power, controlled by the upper of the two circuit breakers, supplies a +5VDC switching power supply, a +12VDC switching power supply, and the cooling fans. +5 and +12 Volt power is individually controlled to each DEC backplane by switches on the Utility panel to provide the capability of shutting down power on a single node, a requirement whenever a DEC logic card is pulled or inserted (loop still functions since the LIU power is separate from the DEC

power). The Utility panel also has eight RUN/HALT switches, one for each of the DEC backplanes, to give further control over the LSI-11. And finally, the Utility panel has a fuse for the cabinet cooling fans. An illustration of the Operator and Utility panels is given in Figure 5.

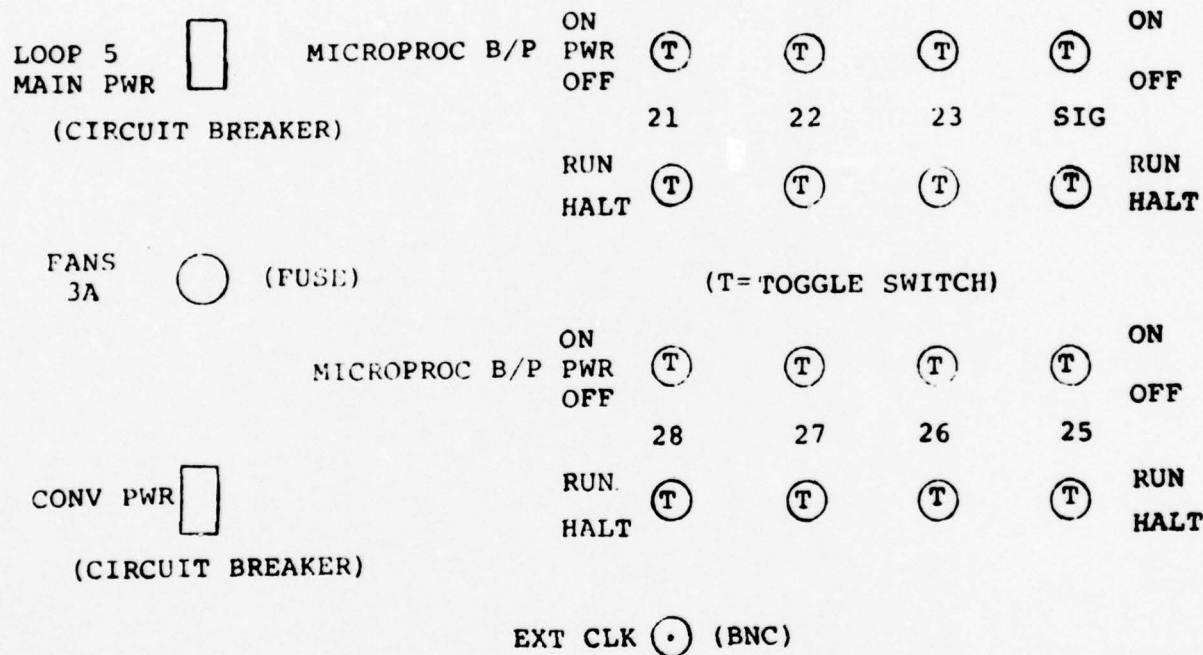
The CPU RUN LEDs are duplicated. Each BLIUI has one built on the board. For the SIG however, there is no BLIUI because there is no loop interface directly between the SIG and the loop, but indirectly through an asynchronous interface (DEC DLV11) from the SIG to an asynchronous interface (DEC DLV11) into the BWBSA function (node 26), and thereby to the loop. For this reason a CPU RUN LED for the SIG is located on the front edge of the BUSCNTL logic card.

Power supplies are located in the bottom of the MSCDM cabinet. Cooling fans are always on when the cabinet power is turned on. Provision has been made for convenience power inside the cabinet since it is expected that maintenance personnel will need receptacles for AC power for their test equipment from time to time.

Five external interfaces exist, relating the MSCDM cabinet to other loops and equipments. Three of these interfaces: the node 21 gateway to Loop 4; the node 28 interface to the Host B processor (PDP11-40); and the node 25 link to the LA36 Printer



OPERATOR PANEL



UTILITY PANEL

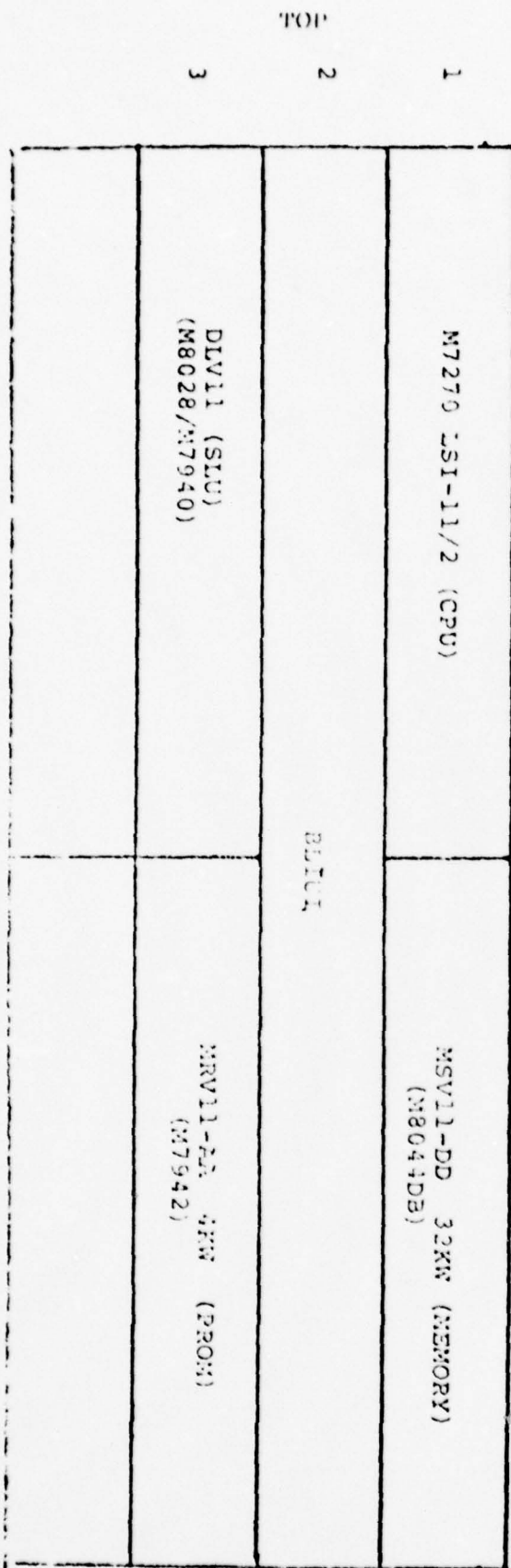
FIGURE 5 CONTROL PANELS

Terminal, use DEC DLV11 asynchronous interface modules to form the DIU. The cabling from these DLV11s to the external world plug into Berg Corp. connectors mounted on the front edge of the DLV11 logic cards. One of the five interfaces, the IEEE Std. 488 (Instrumentation Bus) of node 27 is accomplished by using a DEC IBV11-A logic card specially designed for this type of interface. The cabling from this IBV11-A to the external world plugs into a Berg Corp. connector mounted on the front edge of the IBV11-A logic card. The fifth interface, that of the node 24 Host E (PDP11-V03) is unusual in that it is an interface between the LIU and the BLIUI of node 24. The cable plugs into a connector mounted rigidly to the right lower side of the Burroughs LIU backplane and the cable then runs down to the bottom of the cabinet and out. The connector is wire-wrapped into the LIU backplane.

These are three internal interfaces that run entirely within the cabinet. These interfaces all relate to the Simulated Inputs Generator (SIG). Each interface interconnects DEC DLV11 asynchronous logic cards. The three cable sources are VSQC (node 22), DSQC (node 23), and BWBSA (node 26).

Backplane card positions for the various nodes are given in Figures 6-8.

Clock controls are located on the clock card itself. Two toggle switches are mounted on the front edge. The uppermost switch selects either an external or internal frequency source. Up



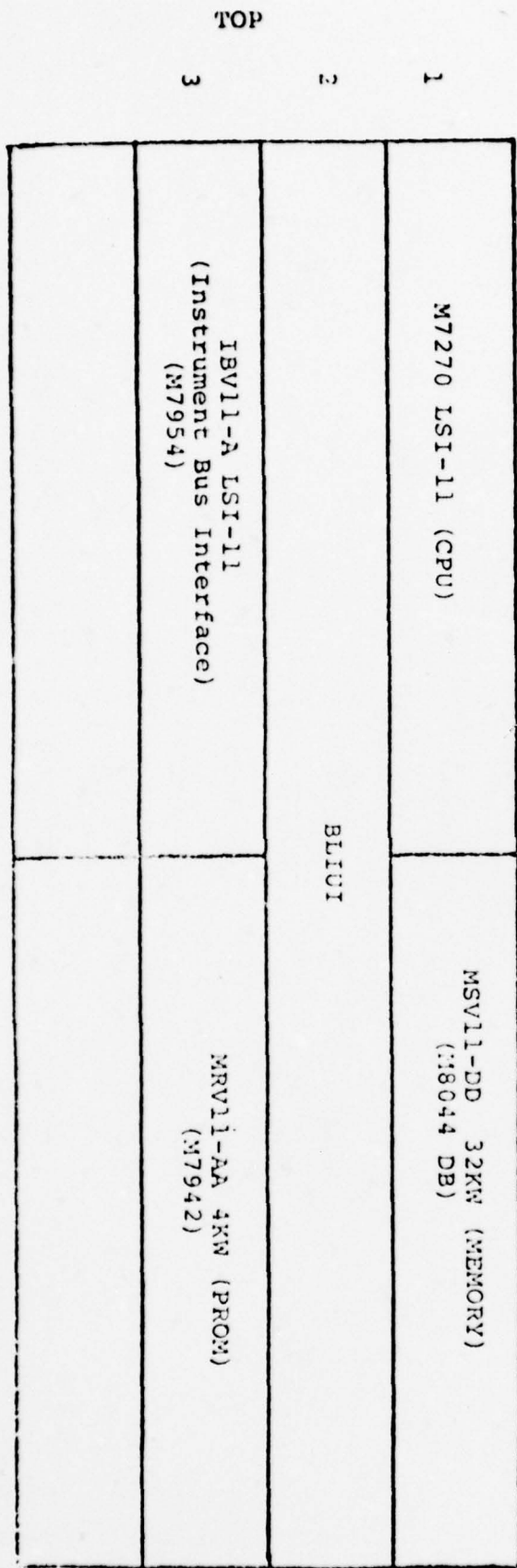
MSCDM

119270 Backplane Card Positions

| | | |
|------|----|-------|
| Node | 21 | SSCI |
| Node | 22 | VSQC |
| Node | 23 | DSQC |
| Node | 25 | OCRI |
| Node | 26 | BWBSA |
| Node | 28 | SDCA |

(Module ID Number)

Figure 6



MSCDM

H9270 Backplane
Card Position FIAC

Node 27 FIAC

(Module ID Number)

Figure 7

TOP

| 4 | 3 | 2 | 1 |
|------------------------------|------------------------------|--------------------------------------|-------------------------|
| MRV11-AA 4KW PROM (M7942) | DLV11 (SLU) (M8028/M7940) | DLV11 (SLU) (M8028/M7940) | LSI-11 (CPU) (M7270) |
| DLV11 (SLU) (M8028/M7940) | DLV11 (SLU) (M8028/M7940) | MSV11-DD 32KW (MEMORY) (M8044 DB) | |

MICROCOMPUTER BACKPLANE

SIG (Simulated Inputs
Generator)

← VIEWING COMPONENTS

Figure 8
Logic Card Placement
(Card insertion view)

position selects internal source (4MHz basic crystal frequency), while the down position selects an external frequency, input via the BNC connector located on the Utility panel (EXT-CLK). The lower switch on the clock card, when in the down position, causes the loop frequency to be divided by two and therefore the loop transmission rate to be one-half the normal rate. With the top switch up (internal source), the clock card divides the fixed internal 4MHz frequency by four to deliver 1MHz to the loop; but with the bottom switch in the down position (1/2 loop rate), the clock is further divided by two before being delivered to the loop. In this case the loop transmission rate will be 500KHz.

Controls on logic cards are given in Figure 9.

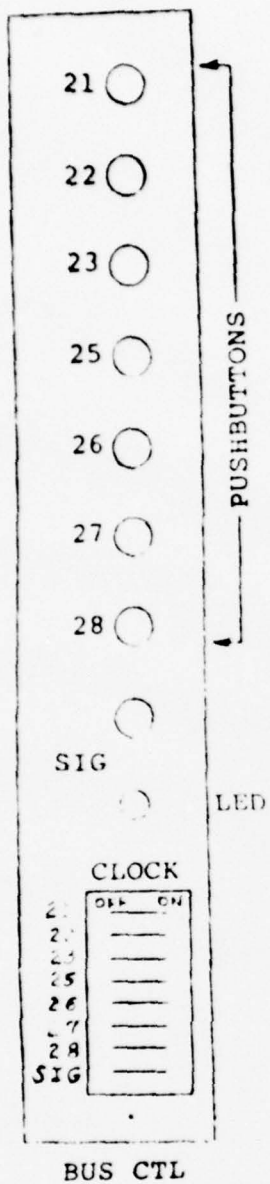


Figure 9 Controls on Logic Cards

3. Software

3.1 MSCDM Functions

The MSCDM functions are described in terms of applications software that is linked to the DMCP and runs on the nine microprocessor modules that make up the MSCDM.

3.1.1 Station to Station Communications Interface (SSCI)

3.1.1.1 Functional Description

The SSCI serves as a gateway node interface to loop 4 of the ESM. It is used to simulate communication between different system control sites. The SSCI performs in-transit queueing and packet routing.

3.1.1.2 Performance Requirements

The SSCI must provide communication (9600 baud) between Loop 5 nodes and other nodes in the ESM.

3.1.1.3 I/O Variables

SSCI receives packets from the loop and its external interface (DLVII).

3.1.1.4 Program Interfaces

The Node 21 software consists of the SSCI application software linked to a modified DMCP which does not do intermediate ACKing. The DMCP (Distributed Master Control Program) is described in Section 3.2 below. The DLV11 interface is controlled by an I/O Handler.

3.1.1.5 Algorithm Utilitization

The SSCI performs the required handshaking to communicate with a loop 4 BDS microcomputer.

3.1.1.6 Exception and Error Conditions

SSCI utilizes the common loop related DMCP exception and error conditions.

3.1.2 Voice Service Quality Control (VSQC)

3.1.2.1 Function Description

The VSQC Module assesses the performance of voice channels to detect degrading performance and assist in fault isolation. Thresholds are compared with fixed performance values for the various channels. Red and alarm values are reported to the Fault Isolations and Control Modules (FIAC).

3.1.2.2 Performance Requirements

The MSCDM must be capable of scanning and monitoring up to 1000 channels per hour.

3.1.2.3 I/O Variables

VSQC Receives measurements from the SIG, and it requests measurements on a specific channel from the SIG. Event reporting ON, OFF and measurement request commands are received from the loop. Red and Amber Event Reports are sent to FIAC via the loop. Measurements are sent to OCRI via the loop.

3.1.2.4 Program Interfaces

The Node 22 software consists of the VSQC application software linked to the DMCP. The DLVll interface to the SIG is controlled by an I/O Handler.

3.1.2.5 Algorithm Utilization

The VSQC performs trending and thresholding on measurement data received from the SIG.

3.1.2.6 Exception and Error Conditions

VSQC utilizes the common loop related DMCP exception and error conditions.

3.1.3 Digital Service Quality Control (DSQC)

3.1.3.1 Functional Description

The DSQC module assesses the performance of digital data channels to detect degrading performance with respect to increasing error rates, and to assist in fault isolation. Bit error rate, pseudo error rate and block error rate for the various channels are input to the DSQC and compared with threshold values. Reports are generated and sent to FIAC.

3.1.3.2 Performance Requirements

The MSCDM must be capable of scanning and monitoring up to 1000 channels per hour.

3.1.3.3 I/O Variables

DSQC receives measurements from the SIG, and it requests measurements on a specific channel from the SIG. Event reporting ON, OFF and measurement request commands are received from the loop. Red and Amber Event Reports are sent to FIAC via the loop. Measurements are sent to OCRI via the loop.

3.1.3.4 Program Interfaces

The Node 23 software consists of the DSQC application software linked to the DMCP. The DLVII interface to the SIG is controlled by an I/O handler.

3.1.3.5 Algorithm Utilization

The DSQC performs trending and thresholding on measurement data received from the SIG.

3.1.3.6 Exception and Error Conditions

DSQC utilizes the common loop related DMCP exception and error conditions.

3.1.4 Data Base Management Service (DBMS) - Program Development Unit (PDU)

3.1.4.1 Functional Description

The DBMS performs the data base maintenance functions. It maintains the display files for the human interface User Language, system configuration files, equipment status files and object files for the various modules. The PDU develops and maintains software for the MSCDM. The PDU may be used as a general purpose processor with mini-disk and local CRT terminal.

3.1.4.2 Performance Requirements

The DBMS must be capable of maintaining status data on 1000 channels, two switches, and three links. It must provide the human interface to MSCDM for up to four ESM-MSCDM terminals.

3.1.4.3 I/O Variables

The DBMS receives terminal inputs from the OCRI nodes and equipment status reports from FIAC and SDCA via the loop. The DBMS writes display information to OCRI and module update commands to VSQC, DSQC, BWBSA, and SDCA via the loop.

3.1.4.4 Program Interfaces

The Node 24 software consists of the six modes of operation of the User Language linked to the DMCP.

3.1.4.5 Algorithm Utilization

The User Language examines loop inputs with respect to source LID, and maintains status on the current dialog position for each remote terminal.

3.1.4.6 Exception and Error Conditions

The User Language informs the OCRI operator of all invalid entries. DBMS also utilizes the common loop related DMCP exception and error conditions.

3.1.5 Operator Control and Report Interface (OCRI)

3.1.5.1 Functional Description

The OCRI interfaces the site operator to the other functional modules at the MSCDM. The User Language interface allows the operator to control the site, request status information concerning site and equipment performance, and to prepare site reports which must be forwarded to other sites. Operator to operator messages are also supported by the User Language. Site and equipment error messages are printed on the OCRI terminal.

3.1.5.2 Performance Requirements

The OCRI must provide the human interface to the MSCDM. The OCRI must be able to be ATTACHED to any node in the 5-ring Multiloop Network.

3.1.5.3 I/O Variables

The OCRI receives data to be displayed on the terminal from the loop. It receives data to be sent on the loop from the terminal keyboard.

3.1.5.4 Program Interfaces

The Node 25 software consists of the OCRI application software

linked to the DMCP. The DLVII interface to the LA36 terminal is controlled by an I/O Handler.

3.1.6 Baseband Signal Analysis and Wide Band Signal Analysis (BWBSA)

3.1.6.1 Functional Description

The BWBSA module performs performance assessment on link equipment. Measurement parameters are compared with threshold values and reports are sent to the Fault Isolation and Control Coordination (FIAC) module. Transmitter, multiplexor and receiver alarms are reported to the FIAC module.

3.1.6.2 Performance Requirements

The BWBSA must be capable of scanning and monitoring three links.

3.1.6.3 I/O Variables

BWBSA receives measurements and alarms from the SIG, and it requests measurements on a specific link from the SIG. Event reporting ON, OFF and measurement request commands are received from the loop. Red and Amber Event Reports and Alarms are sent to FIAC via the loop. Measurements on links are sent to OCRI via the loop.

3.1.6.4 Program Interfaces

The Node 26 software consists of the BWBSA application software linked to the DMCP. The DLVII interface to the SIG is controlled by an I/O Handler.

3.1.6.5 Algorithm Utilization

The BWBSA performs thresholding on measurement data received from the SIG, and recognizes Alarms from equipment.

3.1.6.6 Exception and Error Conditions

BWBSA utilizes the common loop related DMCP exception and error conditions.

3.1.7 Fault Isolation and Control Coordination (FIAC)

3.1.7.1 Functional Description

The Fault Isolation and Control Coordination (FIAC) module interprets Event Reports from measurement function modules and other site FIAC modules for the purpose of isolating the equipment causing the detection of a fault condition. The FIAC displays Event Reports on the OCRI terminal and updates the Status Data Base on DBMS. The FIAC communicates with other FIAC'S and generates Fault Reports to local and remote OCRI's.

The FIAC accepts Event Reports via the loop from VSQC (ND22), DSQC (ND23), and BWBSA (ND26). It also receives Alarm Reports from BWBSA, and Event Reports from a remote FIAC simulated by SDCA (ND28). Outputs include Event and Alarm Reports sent via the loop to the designated OCRI and DBMS (ND24) for Status File updating. Fault Reports are sent to designated Local and Remote OCRIs.

3.1.7.2 Performance Requirements

The FIAC must be capable of processing the inputs from VSQC, DSQC, BWBSA, and another FIAC (simulated by SDCA).

3.1.7.3 I/O Variables

The FIAC accepts Event Reports via the loop from VSQC (ND22), DSQC (23), and BWBSA (26). It also receives Alarm Reports from BWBSA, and Event Reports from a remote FIAC simulated by SDCA (ND28). Outputs include Event and Alarm Reports sent via the loop to the designated OCRI and DBMS (ND24) for Status File updating. Fault Reports are sent to designated Local and Remote OCRIs.

3.1.7.4 Program Interfaces

The node 27 software consists of the FIAC application software linked to the DMCP. The program operates on data from the loop.

3.1.7.5 Algorithm Utilization

The FIAC compares monitor point data from VSQC, DSQC, BWBSA and remote FIAC Event Reports to determine the area of the fault. Additional Red Event Reports to DBMS and OCRI on a specific equipment are suppressed to simulate a hard failure.

3.1.7.6 Exception and Error Conditons

Exception and Error Conditions are common to all nodes running the DMCP; i.e., Primary or Secondary Line Failure, message not ACKed.

3.1.8 Switch Data Collection and Analysis (SDCA)

3.1.8.1 Functional Description

The SDCA module receives switch traffic data generated by switches (e.g., AUTODIN or AUTOVON) and performs loading assessments on this data to detect switch equipment saturation conditions. Error conditions are displayed on the OCRI terminal.

3.1.8.2 Performance Requirements

The SDCA must be capable of monitoring two switches.

3.1.8.3 I/O Variables

SDCA receives measurements from the PDPl1/40 in loop 2, and it requests measurements on a specific switch from the PDPl1/40. Event reporting ON, OFF and measurement request commands are received from the loop. Red Event Reports are sent to OCRI and DBMS via the loop. Measurements on switches are sent to OCRI via the loop.

3.1.8.4 Program Interfaces

The Node 28 software consists of the SDCA application software linked to the DMCP. The DLV11 interface to the PDP11/40 is controlled by an I/O Handler. The PDP11/40 generates random measurement values for the two switches.

3.1.8.5 Algorithm Utilization

The SDCA performs thresholding on measurement data received from the PDP11/40. The SDCA also simulates a remote FIAC by accepting Event Reports, generating Event Reports from another area, and generating remote area Fault Reports.

3.1.8.6 Exception and Error Conditions

SDCA utilizes the common loop related DMCP exception and error conditions.

3.1.9 Simulated Input Generator (SIG)

3.1.9.1 Functional Description

The SIG is a microprocessor that generates simulated channel and link measurement data and alarms to the VSQC, DSQC, and BWBSA modules. In this function it acts as both a communications sensor and a scanner.

3.1.9.2 Performance Requirements

The SIG must be capable of monitoring 1000 channels and 3 links per hour and supplying measurement data over 4-9600 baud asynchronous lines (VSQC, DSQC, BWBSA, and SIG Display Monitor).

3.1.9.3 I/O Variables

The SIG writes measurement data to the VSQC, DSQC, BWBSA, and SIG Display Monitor. It receives requests for measurements from the VSQC, DSQC, and BWBSA.

3.1.9.4 Program Interfaces

The SIG contains I/O Handlers for the four interfaces.

3.1.9.5 Algorithm Utilization

The SIG utilizes random number generation for the measurement data.

3.1.9.6 Exception and Error Conditions

None.

3.2 Distributed Master Control Program

The Distributed Master Control Program (DMCP) resides mainly in the microprocessor (LSI-11) nodes which make up the Burroughs Loop Architecture. DMCP modules which reside in the host computers include a Down-Line Load Module which loads remote microprocessors with memory image object files, an Initialization Module which is used at start-up time, and a System Control Resource Allocation Module which is used for dynamic system reconfiguration. In addition the host computer stores the tables required by the microprocessor for reconfiguration and functional task assignment.

The DMCP can be described in terms of the following modules: Interrupt Handlers, Protocol Modules, Loop Manager, Read and Write Modules, Queue Manager, Command Interpreter, Error Module, and I/O Queues. These functional modules are described below.

The DMCP is an Interrupt or Event Driven System. Events result in interrupts being generated by the external hardware (e.g., Loop Interface Unit - LIU) to the LSI-11 microprocessor. The interrupt results in the execution of a vectored interrupt address which passes program control to an I/O Handler (written in MACRO-11 Assembly Language).

A general understanding of the DMCP can be obtained by examining the flow of control resulting from an event. Figure 3 gives the flow control resulting from a packet being received by the LIU's from the loops. The LIU generates an interrupt to the micro-processor which results in the execution of the LIU Handler. The LIU Handler examines a 16 bit LIU Status Register. Conditions which the LIU Status Register indicates include Buffer 0 or 1 Full, CRC 0 or 1 OK, Input Buffer 0 or 1 Overflow, Line Switch Primary, and Line Switch Backup. Depending on the LIU Status Register value and the information received, control can be passed to three modules. The Error Module will be entered if the LIU status register indicates an error condition (e.g., Line Switch Primary).

An error report will be generated describing the failure. The Loop Protocol Module will be entered and the Packet Header Information will be determined (e.g., sequence number destination and source process ID's). The Loop Address field will also be determined for the process ID of the destination task which accepts reports. Finally the packet will be written to the loop using the Write to Loop Module.

The second control path in Figure 10 will be followed if the input from the ring is a normal type packet destined to the Exodevice (e.g., terminal, minicomputer, data comm line). The Input Q Handler will be entered to link the packet to the Input to

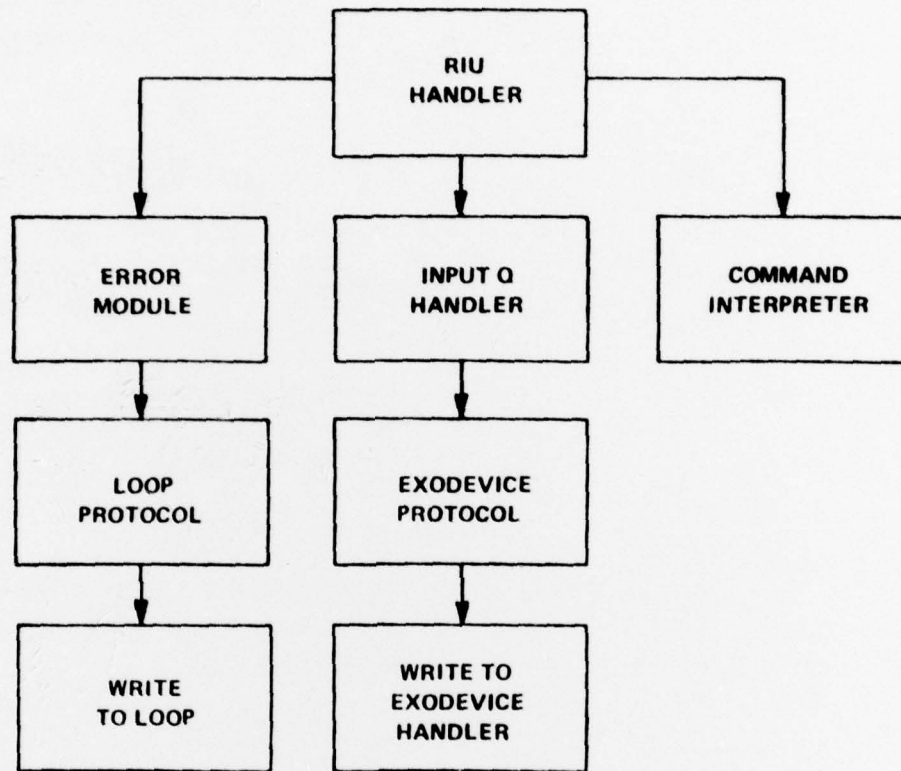


Figure 10 Input from Loop Flow Control

Exodevice Queue. The Exodevice Protocol Module will build the protocol characters for the Exodevice (e.g., SOH, ETX). The Write to Exodevice MOudle will then be called to write the packet.

The third control path will be followed if the control bytes of the header indicate a control path. The Command Interpreter is then entered. Control type commands include ACK's and NAK's, modify loop read address for destructive or non-destructive read, modify reconfiguration and functional task assignment tables, flow control, change write token recognition address, and perform loop-back.

The flow of control for an input from a Exodevice is given in Figure 11. The interrupt results in the execution of the Exodevice Read Handler which can pass control to two modules. A normal loop destined packet will result in the output Q Handler being called. The Loop Protocol Module formats the header of the packet and determines the ring address. The Write to Loop Module writes the packet to the loop.

The second path in Figure 11 results in the Command Interpreter. This module interprets commands originating from the Exodevice. An example would be an ATTACHX command which would be used to logically attach a peripheral connected to the loop to a minicomputer.

The DMCP Idle Flow Control is given in Figure 12. The Input Q Handler is entered to examine the current input queue size. The Output Q Handler is entered to examine whether the packet in the output queue has been ACKed or NAKed. The Loop Manager maintains the watchdog timing function for write token timeouts and retransmission of packets that were not ACKed or NAKed. The System Monitor sends messages to its Exodevice and a System Master to monitor equipment operation.

3.2.1 Interrupt Handlers

Interrupt Handlers are used to process I/O interrupts. The DMCP in each node will contain four basic types. The LIU Handler examines the LIU Status Register and does a Direct Memory Access (DMA) transfer to move a packet (at most 256 bytes) from the LIU buffers to the microprocessor memory. The Clock Handler processes interrupts from the 60 Hz Line Frequency Clock. Interrupts occur every 16.67 msec.; a clock register in memory is incremented at each interrupt. The LIU and Clock Handlers are identical for each node.

A Read and Write Exodevice Handler will be used for each type of Exodevice. Peripheral and data comm handlers will receive interrupts on a per byte basis. Interrupt Handlers will be written in MACRO-11 Assembly Language.

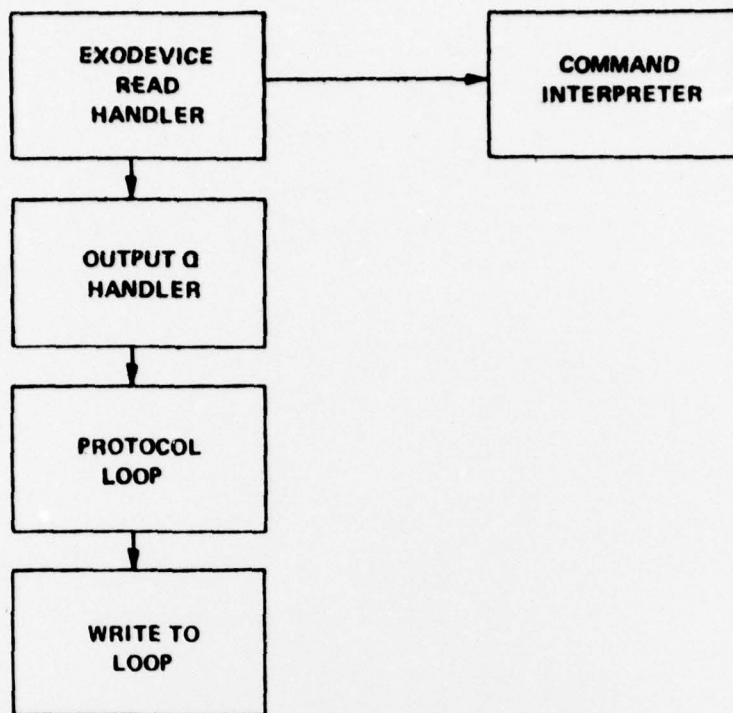


Figure 11 Input from Exodevice Flow Control

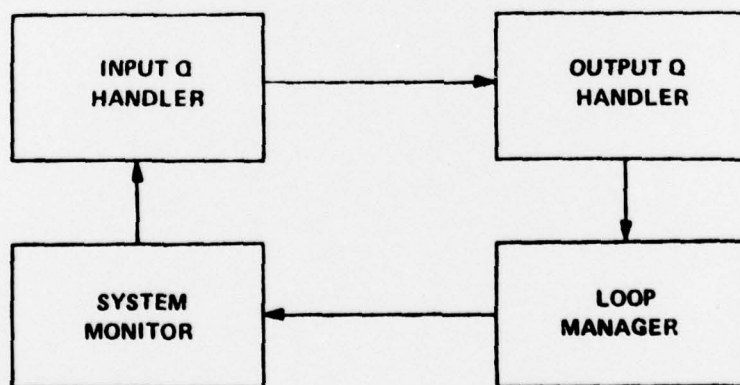


Figure 12 DMCP Idle Flow Control

3.2.2 Protocol Modules

There are two basic types of Protocol Modules; i.e., a Loop Protocol Module and Exodevice Protocol Modules. The Loop Protocol Module is the same at all nodes. Exodevice Protocol Modules are used for each type of exodevice. Protocol Modules format packets, perform code conversion if necessary, and handle communication protocols for the loop, processors, peripherals, and data comm. The Loop Protocol Module determines destination loop addresses based upon its tables for reconfiguration and functional task assignment. Protocol Modules are either separately written in FORTRAN IV or combined with Interrupt Handlers and written in MACRO-11.

3.2.3 Loop Manager

The Loop Manager is written in FORTRAN and is identical for all nodes. It manages certain control functions associated with the loop. One such function is the regeneration of Write Tokens. A Write Token is a special circulating control packet which the LIU must recognize before it can write on the ring. If a Write Token is not received within a certain amount of time, the Ring Manager creates a new Write Token. Another function is the resending of packets to the loop that have not ACKed or NAKed within a certain amount of time.

3.2.4 Read Module

Read Modules will read data from either the loop or an Exodevice. When combined with an Interrupt Handler, Read Modules will be

written in MACRO-11 Assembly Language.

3.2.5 Write Module

Write Modules will write data to the loop or an Exodevice. When combined with an Interrupt Handler, Write Modules will be written in Assembly Language.

3.2.6 Queue Manager

The Queue Manager maintains input and output queues. It maintains status on the number in queue and the current top-of-queue pointer. It moves certain control type command messages to top-of-queue or to other I/O buffers (e.g., intermediate ACK's). The Queue Manager monitors the size of queue and generates flow control command messages. The flow control messages direct nodes to stop sending to a node whose queue is nearly full and resume sending to a node whose queue has emptied. The Queue Manager is used at all nodes. It is written in FORTRAN and interfaces to Interrupt Handlers via COMMON I/O buffers.

3.2.7 Command Interpreter

The Command Interpreter is used to perform nodal control functions as a result of interpreting command packets (utilizing the header control bytes). Many of these command packets such as ACK-NAK's,

line switch, etc. are described above. A function not listed above is Down-Line Loading Command interpretation. A Down-Line Loading command forces the microprocessor to execute a bootstrap loader program stored in PROM memory. The bootstrap loader program loads data coming from the loop into the RAM memory. The data is sent to Absolute Loader Format by the loader host computer (Downline Load Module). The Loader PROM program returns program control to the first executable RAM memory location when an end-of-load command is received. The LSI-11 microprocessor is strapped such that the bootstrap loader PROM is executed at power-up time. The bootstrap loader PROM program is written in Assembly Language.

3.2.8 Error Module

The Error Module is written in FORTRAN and is used at all nodes. The Error Module formats error reports to describe nodal error conditions. These error reports include error conditions indicated by the LIU Status Register (e.g., Loopback), no response from destination nodes, and queue overflow. The reports are sent to a loop connected peripheral.

3.2.9 I/O Queues

I/O Queues are maintained by the Queue Managers. The maximum queue sizes are determined by the speed of the Exodevice Interface, the traffic at the node, and the availability memory (64K bytes maximum). Output to the loop queues are effectively of size

once since each packet is ACKed before the next one is sent. This guarantees that packets are received in the same order as sent and eliminates the need for packet sequencing software.

3.3 User Lanaguage

The User Lanaguage provides the human interface to the MSCDM and controls its operation. It is implemented as a dialogue between a processor and a terminal with displays stored as disk files. It is written to handle four ESM-MSCDM terminals. User language modules are described below:

3.3.1 Mode 1 CRT-to-CRT

This module allows messages to be sent from the MSCDM terminal to the three ESM terminals. In addition to Mode 1, an ATTACH command is provided so that a terminal can connect to another processor or to another terminal. When a terminal is attached to another terminal it can send messages directly without host processor intervention.

3.3.2 Mode 2 System Inquiry

System inquiry allows the MSCDM user to view displays that define the ESM Multiloop Network Simulation Facility. The default display values which correspond to the parameters generated in the nodal software are stored on the mini-disk. Updates to these parameters are stored on the PDP11/40 HSTB in Loop 2. Updates are created via Mode 3 (System Update) of the User Language resident on HSTB. Node designators 20-28 are used for loop 5. The LID/FAD

Conversion Tables are set up such that the FAD is given for the LID for that location on the display.

3.3.3 Mode 3 - Module Update

This mode of operation is used to modify parameters in the other MSCDM nodes. The user is given a list of parameters that may be changed. The parameter changes are performed in the remote nodes by special control packets that are generated by DBMS.

3.3.4 Mode 4 - File Access

This mode of operation allows records of files to be accessed, modified, added and deleted. The files are the circuit and trunk files.

3.3.5 Mode 5 - Report

This mode of operation is used to generate the system control reports. The operator is led through a menu-selection dialogue. This dialogue first asks whether a file is already open so that the operator can exit from mode 5 and return to complete the report later. Two types of reports can be generated: channel-link and switch. The user is prompted for the various elements of the report and the format of the response. A list of remarks can be added to the report. Simulation of a report being sent to a different System Control hierarchical level via the ASSCI gateway node is done by entering the node designator of an ESM node. The report can then be sent to an ESM terminal or host processor.

3.3.6 Mode 6 - Status

This mode of operation displays the status of simulated equipment that is being monitored by MSCDM.

3.4 System Utilities

The following utilities which run on the PDU were developed for the MSCDM application.

3.4.1 Loader

The loader utility (FDMLDR) is used for loading the remote LSI-11 microprocessors via the loop. The loader utility is used in conjunction with the Loader PROM program at each node contained on its PROM card.

3.4.2 Page Print

The page print utility (PAGE) allows the use of the LA36 Loop Connected OCRI terminal as a line printer so that listings can be made for the PDU.

3.4.3 User Language File Format

The user language file format utility (MSGCON) formats EDI files into 80 byte source records for utilization with the user language.

3.5 Diagnostics

Diagnostics developed for isolating bad cards for loop 5 nodes include:

LIUBUF - for testing the LIU I/O buffers

LIURAM - for testing the address comparison memory on the LIU

LSICPU - for testing the LSI-11 processor

LSIMEM - for testing the LSI-11 memory

LIUINT - for testing the LIU/LSI-11 (BLIUI) interface card.